EP 0 844 649 A2

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 844 649 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.05.1998 Bulletin 1998/22

(51) Int. Cl.[6]: **H01L 21/306**

(21) Application number: **97120374.0**

(22) Date of filing: **20.11.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **20.11.1996 JP 308842/96**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

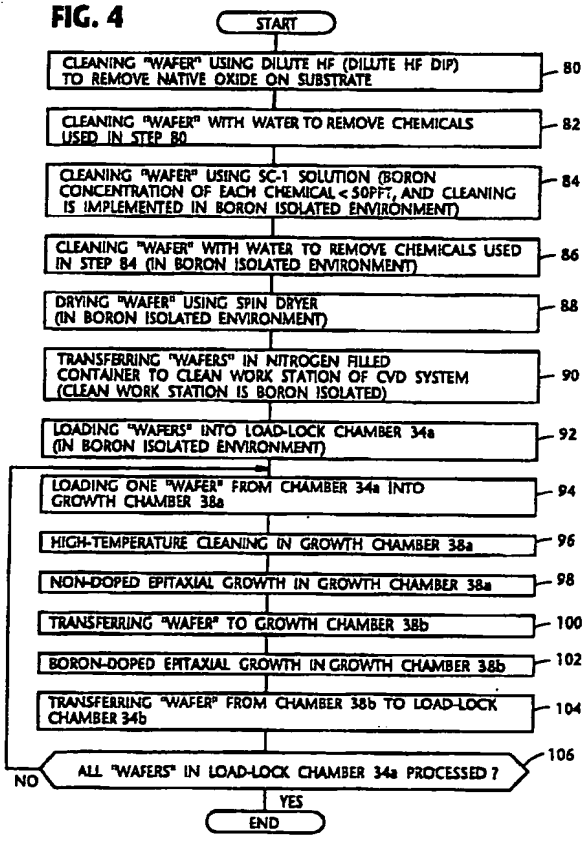
(72) Inventors:
- **Suzuki, Tatsuya**
  Minato-ku, Tokyo (JP)
- **Aoyama, Tohru**
  Minato-ku, Tokyo (JP)

(74) Representative:
Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) A method for boron contamination reduction in IC fabrication

(57) In order to reduce boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, the silicon substrate is pre-treated, before being loaded into the CVD apparatus, such as to prevent the substrate from being contaminated by boron in a clean room. Further, in accordance with one embodiment, a CVD growth chamber itself is cleaned, before the substrate is loaded into the growth chamber, using an F_2 gas at a predetermined temperature of the substrate, thereby to remove boron residues in the growth chamber;

FIG. 4



EP 0 844 649 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to semiconductor device fabrication techniques using ULSI (ultra-large-scale integration) technology, and more specifically to a method of effectively lowering boron (B) concentration at an interface between an epitaxially grown film and the Si substrate surface. Such a film may be a Si or $Si_{1-x}Ge_x$ film selectively deposited in an UHV-CVD (ultrahigh vacuum/chemical vapor deposition) apparatus using a source gas(es) such as SiH_4, Si_2H_6, GeH_4, etc.

2. Description of the Related Art

It is known in the art that the selective epitaxial growth of Si or $Si_{1-x}Ge_x$ on a silicon wafer surface, using an UHV-CVD apparatus with a source gas(es) such as SiH_4, Si_2H_6, or GeH_4, has found an extensive application in forming about 0.1 μm level of channel epitaxial construction in a miniaturized MOS (metal-oxide semiconductor) transistors, next generation's high-speed bipolar transistors, etc.

Before turning to the present invention, it is deemed advantageous to describe, with reference to Figs. 1(A)-1(C), 2, and 3, conventional techniques relating to the present invention. Throughout the instant disclosure, term "substrate" is interchangeably used with "wafer". Although a high-speed bipolar transistor is referred to in this specification, it should be noted that the present invention is in no way limited thereto.

Figs. 1(A)-1(C) are schematic cross-sectional views depicting the fabrication of a high-speed NPN bipolar transistor. In brief, a substrate wherein a collector portion has been formed as shown in Fig. 1(A), is transferred to an UHV-CVD apparatus such as that is schematically shown in Fig. 2. In the UHV-CDV apparatus, a Si or $Si_{1-x}Ge_x$ epitaxial base portion is grown on the substrate as illustrated in Fig. 1(B). Following this, the wafer (or substrate) is removed from the UHV-CVD apparatus and an emitter portion is formed on the substrate in the manner shown in Fig. 1(C).

The present invention is directed to effective reduction of boron contamination (or concentration) at an interface between an epitaxially grown film and the Si substrate surface. To this end, each wafer is pretreated before being loaded into the CVD apparatus, and/or a growth chamber of the CVD apparatus is cleaned prior to each CVD process. Thus, it will be understood that the formation of the emitter portion shown in Fig. 1(C) is not relevant to the present invention.

Referring to Fig. 1(A), an N^+ layer 10 is grown on an P^+(100)-oriented Si substrate 12 with resistivity ranging from 10 to 20Ωcm (for example). Following this, an N^- epi-layer 14, which functions as a collector, is deposited on the N^+ layer 10. Further, as illustrated in Fig. 1(A), a SiO_2 layer 16, a P^- poly-Si layer 18, and another SiO_2 layer 20 are successively formed using conventional lithography and etching techniques.

The substrate, which has undergone the above processes, is transferred to the UHV-CVD apparatus wherein the Si or $Si_{1-x}Ge_x$ epitaxial base (denoted by numeral 22) is selectively grown on the N^- epi-layer 14. In this case, inner portions of the poly-Si layer 18 grow downwardly as schematically shown in Fig. 1(B). Subsequently, the substrate shown in Fig. 1(B) is unloaded from the UHV-CVD apparatus, after which a SiO_2 layer 24 and an N^+ poly-Si emitter layer 26 are formed, as shown in Fig. 1(C), using conventional techniques. The processes for forming the structure shown in Figs 1(A)-1(C) are well known and not directly concerned with the present invention, and thus further description thereof will be omitted for brevity.

Fig. 2 is a diagram schematically showing one example of an UHV-CVD apparatus (denoted by numeral 30), which comprises a robotic transfer section 32, two load-lock chambers 34a and 34b, another robotic transfer section 36, and two growth chambers 38a and 38b. The UHV-CVD apparatus 30 per se is well known in the art. Other sections such as turbo pumps, which are irrelevant to the present invention, are not shown in Fig. 2 for the sake of simplifying the disclosure. Fig. 2 will also be referred to in the preferred embodiments of the present invention.

The robotic transfer section 32 comprises a clean bench 40 and two substrate transfer robots 42a and 42b, while the robotic transfer section 36 includes a similar substrate transfer robot 44,

Each of the substrates or wafers, which has been processed as shown in Fig. 1(A), is cleaned and then disposed in a substrate carry box 46a which is, in this case, positioned in a place other than on the clean bench 40. This box 46a is then transported to the clean bench 40, as illustrated in Fig. 2. The precleaned wafers contained in the box 46s are loaded on a one-by-one basis, using the robot 42a, into the load-lock chamber 34a. After all the wafers in the box 46a are loaded into the load-lock chamber 34a, the chamber 34a is pumped down to a predetermined pressure. Once the predetermined pressure is reached, the first wafer in the load-lock chamber 34a is introduced, by way of the robot 44, into the growth chamber 38a which is dedicated to non-doping epitaxial growth.

After the epitaxial growth is completed in the chamber 38a, the wafer is conveyed to another growth chamber 38b which is dedicated to p-type (viz., B) doping epitaxial growth. The reason why the two growth chambers 38a and 38b are used will be described later. When the film deposition on the wafer at the chamber 38b is finished, the wafer is transferred to the load-lock chamber 34b. These processes are repeated with each of the wafers stored in the load-lock chamber 34a.

When all the wafers in the load-lock chamber 34a are processed and loaded into the other load-lock chamber 34b, they are placed into another substrate carry box 46b by the robot 42b. The wafers in the box 46b are then transported to the next wafer process station, wherein subsequent wafer treatments, such as referred to with respect to Fig. 1(C), are implemented.

Fig. 3 is a flow chart depicting the steps that characterize the conventional processes which include cleaning and CVD processes. In more specific terms, the Si wafers, on which layers or films shown in Fig. 1(A) are formed, are precleaned and then transferred to the UHV-CVD apparatus 30 shown in Fig. 2.

Referring to Fig. 3, at step 50, each Si wafer undergoes a dilute HF (hydrofluoric acid) dip in order to remove native oxide formed on the wafer, after which the chemicals used in step 50 are removed by water washing (step 52). Immediately thereafter, at step 54, the wafer is subjected to a well known RCA cleaning process using a cleaning solution, NH_4OH (ammonia)-H_2O_2 (hydrogen peroxide)-H_2O (pure water), thereby removing particles and organic contaminations on the wafer. The cleaning with the aforesaid solution is called "standard cleaning 1 (SC-1)), at NH_4OH-H_2O_2-H_2O (=1:1:5) (for example) at 60 to 80°C for 3 to 10 minutes. Following this, at step 56, the reagents used in step 54 are washed away using pure water, and the wafer is then dried using a spin dryer (step 58). The above mentioned wafer cleaning is carried out with each of a predetermined number of the wafers. Subsequently, the precleaned Si wafers are accommodated in the box 46a (Fig. 2) and transported to the clean bench 40 of the UHV-CVD apparatus 30 (Fig. 2).

The Si wafers in the wafer carry box 46a are then successively loaded into the load-lock chamber 34a (step 60). At step 62, a first wafer in the load-lock chamber 34a is loaded into the growth chamber 38a by way of the wafer transfer robot 44. When the first wafer is placed in the growth chamber 38a, the chamber is pumped down to a pressure of 10^{-9} to 10^{-10} torr. At step 64, the wafer is subjected to a high-temperature treatment (viz., high-temperature flashing) in the growth chamber 38a at more than 900°C for about 5 minutes in order to remove the native oxide on the wafer. At step 66, a temperature of the wafer is lowered to 600-800°C, after which selective Si or $Si_{1-x}Ge_x$ non-doped epitaxial growth is carried out on the wafer using a source gas(es) selected among SiH_4, Si_2H_6, GeH_4, etc. as is well known in the art.

Subsequently, the flow proceeds to step 68 whereat the wafer is transferred to the growth chamber 38b. At step 70, a boron-doped selective Si or $Si_{1-x}Ge_x$ epitaxial growth is implemented on the wafer, wherein diborane (B_2H_6) is used as a dopant gas for forming a p-type base layer. In the above, the wafer is transferred from the chamber 38a to the chamber 38b in a vacuum environment thus obviating the need for implementing the high-temperature flashing on the wafer in the growth chamber 38b. At step 72, the wafer on which the p-type base layer has been grown is loaded into the load-lock chamber 34b. Thereafter, the next wafer in the load-lock chamber 34a is introduced into the growth chamber 38a from the load-lock chamber 34a and is subjected to the above mentioned processes. At step 74, a check is made to determine if all the wafers in the load-lock chamber 34a are processed. If the answer to the inquiry made at step 74 is affirmative (viz., YES), the flow shown in Fig. 3 is terminated.

The above mentioned known wafer processing steps, however, suffer from the problem that the selective Si or $Si_{1-x}Ge_x$ epitaxial growth on the wafer undesirably leaves "boron contamination" at the boundary between the epitaxial layer and the substrate surface. The boron concentration typically exhibits more than 1E17 (i.e., 1×10^{17}) atoms/cm^3 at peak concentration and 1E12 atoms/cm^2 at sheet concentration. The causes of such a high boron concentration are as follows.

(1) Boron is contained in the cleaning solution used in the RCA cleaning process. For example, in the case where the solution is a composition of Ammonia-"Hydrogen Peroxide"-"pure water"=1:1:5, boron in the order of about 100ppt (parts per trillion) is present in the above-mentioned standard cleaning (SC-1) solution. Thus, when a wafer is subjected to the conventional RCA cleaning, boron is undesirably absorbed into or included in the native oxide.

(2) In the clean room, the filtered air flows from ceiling to floor. Such a filter ceiling system includes a borosilicate glass fiber filter such as UPA (ultra low penetration air) filter, HEPA (high efficiency particulate air) filter, etc. The descending airflow contains boron resulting from the glass fiber filters. Further, these filters are unable to successfully strain out boron which is contained in the outside (viz., open) air which is introduced to the clean room. As a result, boron is inherently present in the clean room environment. Thus, the boron concentration in the SC-1 solution is further enhanced with the result of additional boron being taken into the native oxide. Still further, during the steps 50, 52, 56, 58 and 60 (Fig. 3), boron tends to adhere, in the clean room environment, to the native oxide developed on the wafer.

(3) Boron which is adhered to the native oxide remains on the wafer even if the native oxide is removed by the high-temperature flashing in the growth chamber.

The above mentioned high boron concentration at the interface between the epitaxial layer and the surface of the Si water, undesirably lowers a cut-off frequency of a high-speed bipolar transistor, and causes variation of the threshold voltage in the case of miniaturized CMOS transistors.

One approach to reducing the boron contamination is disclosed in Japanese Laid-open Patent Application No. 4-97517. According to this prior art, a wafer which has been subjected to the RCA cleaning is treated using dilute HF and then cleaned using water whereby boron is removed as BF_3. The prior art, however, has encountered the difficulty that the surface of the wafer is exposed to an ambient clean room atmosphere and thus, the wafer is susceptible to organic and/or inorganic contamination which cannot be removed even by the high-temperature flashing in the growth chamber.

SUMMARY OF THE INVENTION

It is therefore an object of the present to effectively reduce boron concentration between a silicon substrate and a Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus.

One aspect of the present invention resides in a method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of: (a) cleaning the substrate using a solution including a plurality of chemicals each of which contains boron whose concentration is less than 50 ppt, the cleaning being implemented before the substrate is loaded into the CVD apparatus; and (b) processing the substrate in a boron-free isolated environment at step (a) and before the substrate is loaded into the CVD apparatus.

Another aspect of the present invention resides in a method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of: (a) ion implanting silicon atoms into the substrate before the substrate is loaded into the CVD apparatus; (b) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus; and (c) implementing a high-temperature treatment on the substrate in the CVD apparatus thereby diffusing boron, adhered to the substrate, into the substrate.

Still another aspect of the present invention resides in a method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of: (a) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus; (b) removing native oxide produced on the substrate at step (a) using a dilute HF before the substrate is loaded into the CVD apparatus; (c) immersing the substrate in boiling concentrated HNO_3 to form native oxide on the substrate; the immersing of the substrate being implemented before the substrate is loaded into the CVD apparatus; and (d) implementing a high-temperature treatment on the substrate in the CVD apparatus to diffuse boron, adhered to the substrate, into the substrate.

Still another aspect of the present invention resides in a method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of: (a) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus; (b) removing native oxide produced on the substrate at step (a) using a dilute HF before the substrate is loaded into the CVD apparatus; (c) growing thermally oxide on the substrate using an oxygen gas in a low-pressure atmosphere before the substrate is loaded into the CVD apparatus; and (d) implementing a high-temperature treatment on the substrate in the CVD apparatus to remove the oxide which has thermally been grown on the substrate at step (c).

Still another aspect of the present invention resides in a method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of: (a) cleaning a CVD growth chamber, before the substrate is loaded into the growth chamber, using an F_2 gas at a predetermined temperature of the substrate, thereby to remove boron residues in the growth chamber; (b) implementing a high-temperature treatment on the substrate loaded into the growth chamber to remove native oxide on the substrate; and (c) implementing sequentially non-doped and boron-doped epitaxial growths on the substrate in the growth chamber.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become more clearly appreciated from the following description taken in conjunction with the accompanying drawings in which like elements are denoted by like reference numerals and in which:

Figs. 1(A) to 1(C) are cross-sectional views each showing film depositions while forming a high-speed bipolar transistor, having referred to in the opening paragraphs of the instant disclosure;

Fig. 2 is a diagram showing a conventional UHV-CVD apparatus;

Fig. 3 is a flow chart which includes steps of part of bipolar transistor fabrication;

Fig. 4 is a flow chart which includes steps which characterize the first embodiment of the present invention;

Figs. 5(A) and 5(B) are each showing a clean work station used in the first embodiment;

Fig. 6 is a diagram showing a conventional UHV-CVD which is equipped with a clean work station according to the present invention;

Fig. 7 is a flow chart which includes steps which characterize the second embodiment of the present invention;

Figs. 8(A) and 8(B) are diagrams which show thermally grown oxide on the substrate and a manner of ion implantation, respectively;

Figs. 9(A) and 9(B) are each showing a flow chart which includes steps which characterize the third embodiment of the present invention;

Fig. 10 is a flow chart which includes steps which characterize the fourth embodiment of the present invention;

Fig. 11 is a flow chart which includes steps which characterize the fifth embodiment of the present invention;

Fig. 12 is a diagram showing an UHV-CVD used with the fifth embodiment; and

Fig. 13 is a graph which shows the experiments results of the first to fourth embodiments together with the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the present invention will be described with reference to Figs. 4-6.

In order to simplify the instant disclosure, it is assumed that the silicon substrates (or wafers), on each of which the layers shown in Fig. 1(A) has already been formed, are cleaned and then transferred to an UHV-CVD apparatus (or system) 31 shown in Fig. 6. Further, as mentioned above, a $Si_{1-x}Ge_x$ (or Si) layer is formed on each wafer in the CVD apparatus 31. This CVD apparatus 31 is identical with the apparatus 30 of Fig. 2 except that the robotic transfer section 32 is substantially isolated from the ambient clean room atmosphere. Thus, the portions of Fig. 6, which are identical with those of Fig. 2, are indicated by the same numerals as used in Fig 2.

As shown in Fig. 4, at step 80, each silicon wafer undergoes dilute HF (hydrofluoric acid) dipping in order to remove native oxide formed on the wafer. Thereafter, the chemicals or reagents used in step 80 are removed by washing each wafer using water (step 82). Steps 80 and 82 are essentially identical with steps 50 and 52 of Fig. 3, respectively. The wafer is then cleaned, without being dried, using "standard cleaning 1 (SC-1) solution" of the RCA cleaning process (viz., NH_4OH-H_2O_2-H_2) for removing particles and organic contaminants (impurities). The standard cleaning (SC-1) solution is composed of NH_4OH-H_2O_2-H_2 (typically 1:1:5) in this case and its temperature is maintained at about 70°C. By the way, the solution is also referred to as APM (Ammonia-Hydrogen Peroxide Mixture). It should be noted that boron concentration of each of ammonia (NH_4OH), hydrogen peroxide (H_2O_2), and pure water is selected to be less than 50ppt.

Further, the wafer cleaning using the SC-1 solution is implemented in a clean work station 110 (Figs. 5(A) and 5(B)) which is provided in a conventional clean room. Reference is now made to Figs. 5A and 5B, which are respectively a perspective and cross-sectional views of the clean work station 110. In Fig. 5B, arrows indicate air flow. The station 110 is provided with a clean bench 112 therein, on which a container of the SC-1 solution is placed. More specifically, the clean work station 110 is comprised of one or more air intake fans 114 by which air in the clean room is introduced into the station 110. Further, the station 110 includes a chemical filter 116 which has an effective boron adsorptive power. The interior of the clean work station 110 is isolated from the clean room by way of a curtain 118 of vinyl chloride. One side of the curtain 118 is provided with a zipper or slide fastener 120 for the purpose of access to the inside of the station 110.

Returning to Fig. 4, at steps 86 and 88, the wafers are cleaned with water and then dried using a conventional spin dryer. These wafer treatments are carried out on the clean bench 112 within the station 110 shown in Fig. 5B. At step 90, the precleaned wafers are accommodated in a wafer carry box filled with nitrogen and then transferred to the clean bench 40 of the robotic transfer section 32 (Fig. 6). This section 32 is also isolated from the clean room in order to prevent boron traces in the clean room from entering the section 32. That is, the robotic transfer section 32 is provided in a clean work station similar to that shown in Figs. 5A and 5B, a manner of which is indicated by a bold line 33. In this case, it is necessary to provide openings for loading the wafers into the load-lock chamber 34a and for unloading the wafers into another load-lock chamber 34b. The above mentioned wafer carry box, which is filled with nitrogen, is indicated by 46a' in Fig. 6.

The silicon wafers in the box 46a' are then successively loaded into the load-lock chamber 34a (step 92) in a boron-free isolated environment. At step 94, a first wafer in the load-lock chamber 34a is transferred into the growth chamber 38a by way of the wafer transfer robot 44. When the first wafer is placed in the growth chamber 38a, the chamber 38a is pumped down to a pressure of 10^{-9} to 10^{-10} torr (for example). At step 98, the temperature of the wafer is raised to about 950°C and undergoes a high-temperature treatment (viz., high-temperature flashing) for about 5 minutes in order to remove native oxide on the wafer. Immediately after the high-temperature treatment on the wafer is completed, the temperature of the wafer is lowered to about 700°C. At step 98, a non-doped epitaxial Si layer with a thickness of about 2000 angstrom (for example) is selectively grown on the wafer, as shown in Fig. 1B, while flowing a Si_2H_6 gas into the chamber 38a at a rate of 10 sccm (standard cm^3/min). As an alternative, a non-doped $Si_{1-x}Ge_x$ epitaxial layer may be grown using source gases of Si_2H_6 (or SiH_4) and GeH_4.

Subsequently, at step 100, the wafer is transferred to another growth chamber 38b. At step 102, a boron-doped Si layer is grown on the non-doped layer in the chamber 38b using diborane (B_2H_6) as a dopant gas for forming a p-type base layer. In the above, the wafer is

transferred from the chamber 38a to the chamber 38b in a vacuum environment and thus, there is no need for implementing the high-temperature flashing in the growth chamber 38b. At step 104, the wafer on which the p-type base layer has been grown is leaded into the load-lock chamber 34b. Thereafter, the next wafer in the load-lock chamber 34a is introduced into the growth chamber 38a from the load-lock chamber 34a and is subjected to the above mentioned processes. At step 106, a check is made to determine if all the wafers in the load-lock chamber 34a are processed. If the answer to the inquiry made at step 106 is affirmative, the flow shown in Fig. 4 is terminated.

According to experiments conducted by the inventors, under the conditions as mentioned above, the peak concentration of boron at an interface, between the epitaxial layer and the substrate, was 4E16 atoms/cm^3. On the other hand, the sheet concentration of boron at the same interface was 1E11 atoms/cm^2. On the contrary, in the case where the above mentioned boron isolation in the clean room was not implemented at steps 84, 86, 88, 90, and 92, the peak concentration of boron at the interface was 3E17 atoms/cm^3. Further, the sheet concentration of boron at the interface was 1E12 atoms/cm^2. These results were obtained using the above-mentioned secondary-ion mass spectroscopic (SIMS) technique and are plotted in Fig. 13.

Further, as the concentration of boron at the interface between the epitaxial layer and the substrate can effectively be reduced, it is expected to be able to improve a cutoff frequency of a bipolar transistor to a considerable extent.

A second embodiment of the present invention will be described with reference to Figs. 2, 7, 8(A) and 8(B). In the second embodiment, the boron isolating means such as the clean work station 110 of Figs. 5(A) and 5(B) is not used,

As in the first embodiment, assuming that the silicon substrates (or wafers), on each of which the layers shown in Fig. 1(A) has already been formed, are pretreated and then transferred to UHV-CVD apparatus (or system) 30 shown in Fig. 2.

As shown in Fig. 7, at step 200, a thermally grown silicon oxide is formed on the substrate using a conventional process. This thermally grown oxide on the substrate is schematically illustrated by numeral 201 in Fig. 8(A), and has a thickness of about 200 angstrom (for example). At step 202, silicon ions are implanted at the conditions of 10 KeV and 1E13 atomes/cm^2 (for example). Fig. 8(B) shows schematically the manner of ion implantation. Further, at step 204, the water is cleaned using a dilute HF solution in order to completely remove the thermally grown oxide. Subsequently, the wafer is subjected to cleaning with water (step 206), cleaning using the SC-1 solution (step 208), cleaning with water (step 210), and drying using a spin dryer (212), all of which correspond to steps 82, 84, 86, and 88 of Fig. 4. However, as mentioned above, the clean work station 110 of Figs. 5(A) and 5(B) is not used in the second embodiment. That is, the aforesaid steps of Fig. 7 are implemented in the clean room environment. Thereafter, at step 214, the pretreated wafers are accommodated in a wafer carry box filled with nitrogen and then transferred to the clean bench 40 of the robotic transfer section 32 (Fig. 2). It is to be noted that the above mentioned wafer carry box, which is filled with nitrogen, is not shown in Fig. 2 but corresponds to the box 46a. The silicon wafers in the box 46a are then successively loaded into the load-lock chamber 34a (step 216). The following steps 218, 220, 222, 224, 226, 228, and 230 are respectively identical with the steps 94, 96, 98, 100, 102, 104, and 106 of Fig. 4, and accordingly, further description thereof will not be given for simplifying the instant disclosure.

In the above, the process of growing thermal oxide at step 200 may be omitted, in the case of which step 204 is also omitted.

According to the second embodiment, at step 208, native oxide is formed on the substrate while cleaning the wafer using the SC-1 solution. However, boron introduced into native oxide or adhered to the surface thereof during the process at step 208 is diffused in an accelerated manner into the substrate while the wafer is subjected to the high-temperature flashing at step 220. This is because large quantities of interstitial Si atoms are produced during the silicon implantation. Further, the implant damage is removed at steps 208 and 220. For further details of the aforesaid boron diffusion into the silicon substrate, reference should be made to, for example, a paper entitled "Trap-limited interstitial diffusion and enhanced boron clustering in silicon" by P.A. Stolk, et al., App. Phys. Lett. 66(5), 30 January 1995, pages 568, 570.

In connection with the second embodiment, according to experiments conducted by the inventors under the conditions as mentioned above, the peak concentration of boron at an interface between the epitaxial layer and the substrate was 3.5E16 atoms/cm^3. On the other hand, the sheet concentration of boron at the same interface was 8E10 atoms/cm^2. These results were obtained using the above-mentioned secondary-ion mass spectroscopic (SIMS) technique and are also shown in Fig. 13.

A third embodiment of the present invention will be described with reference to Figs. 2, 9(A) and 9(B). In the third embodiment, the boron isolating means such as the clean work station 110 of Figs. 5(A) and 5(B) is not used.

As in the first embodiment, it is assumed that the silicon substrates (or wafers), on each of which the layers shown in Fig. 1(A) has already been formed, are pretreated and then transferred to an UHV-CVD apparatus (or system) 30 shown in Fig. 2.

As shown in Fig. 9(A), at step 300, the wafer is cleaned using a dilute HF solution for removing native oxide on the substrate. Subsequently, the wafer is sub-

jected to cleaning with water (step 302), cleaning using the SC-1 solution (step 304), and cleaning with water (step 306), all of which correspond to steps 82, 84, 86, and 88 of Fig. 4. However, as mentioned above, the clean work station 110 of Figs. 5(A) and 5(B) is not used in the third embodiment. That is, the above steps of Fig. 9(A) are implemented in the clean room environment.

Thereafter, at step 308, the wafer is again cleaned using dilute HF to remove native oxide on the wafer, which is produced in step 304, after which at step 310 the water is washed with water to remove the chemicals used in the previous step 308. Following this, at step 312, the wafer is immersed (or cleaned) in boiling or hot concentrated HNO_3 (nitric acid) in order to again develop native oxide (about 15 angstrom in thick) on the substrate. Thereafter, the wafer is cleaned with water (step 314), after which, at step 318, the thickness of the native oxide is reduced to about 5 angstrom using dilute HF ≦ about 1%. At step 320, the wafer is dried using a spin dryer. The following steps 322 to 338 are respectively identical with the corresponding steps 214 to 230, and accordingly, further description thereof will not be given for simplifying the instant disclosure.

Since nitric acid contains no boron, the native oxide grown at step 312 contains very little boron compared to the native oxide produced when a wafer is cleaned using the SC-1 solution at step 304. Further, the thickness of the native oxide produced at step 312 is reduced and thus, only a thin native oxide layer containing almost no boron remains on the substrate and is removed in the high-temperature flashing in step 328 as in the previous embodiments.

In the above, however, if the thickness of the native oxide can be controlled such as to be sufficiently small as referred to in connection with step 316, the operation at step 316 can be omitted,

In connection with the third embodiment, according to the experiment conducted by the inventors under the conditions as mentioned above, the peak concentration of boron at an interface between the epitaxial layer and the substrate was 3.0E16 atoms/cm^3. On the other hand, the sheet concentration of boron at the same interface was 6E10 atoms/cm^2. These results were obtained using the above-mentioned secondary-ion mass spectroscopic (SIMS) technique and are plotted in Fig. 13.

A fourth embodiment of the present invention will be described with reference to Figs. 2 and 10. In the fourth embodiment, the boron isolating means such as the clean work station 110 of Figs. 5(A) and 5(B) is not used.

As in the first embodiment, it is assumed that the silicon substrates (or wafers), on each of which the layers shown in Fig. 1(A) has already been formed, are pretreated and then transferred to an UHV-CVD apparatus (or system) 30 shown in Fig. 2.

Steps 400 to 410 in Fig. 10 are respectively identical with steps 300 to 310 of Fig. 9(A) and accordingly, these steps will not been described for the cake of brevity. At step 412, the wafer is dried using a spin dryer. Thereafter, at step 414, silicon oxide is thermally grown on the substrate using an oxygen gas in a low-pressure environment. The subsequent steps 416 to 432 are respectively identical to steps 322 to 338 of Fig. 9(A) and thus, further description thereof will be omitted for simplifying the instant disclosure.

In the above, the thermal oxide growth is implemented at less than 20 torr in a CVD growth chamber. In this case, the temperature of the substrate is equal to or less than 900°C. Further, the thermally grown oxide has a thickness of being equal to or less than 30 angstrom.

The thermally grown oxide on the substrate under a reduced pressure environment contains almost no boron. Further, such an oxide is highly compacted in structure (viz., compact substance) compared with native oxide grown on the substrate due to the cleaning using the SC-1 solution and thus, it is difficult that boron in the clean room adheres to the oxide grown in step 414.

In connection with the fourth embodiment, the inventors conducted experiments under the process conditions wherein (a) the thermal oxide growth was implemented at 10 torr in a CVD growth chamber, (b) the temperature of the substrate was kept at 900°C, and (c) the thermally grown oxide has a thickness of 20 angstrom. Further, the conditions of the CVD apparatus were set as mentioned in the first embodiment. The experiment results showed that the peak concentration of boron at an interface between the epitaxial layer and the substrate was 2.5E16 atoms/cm^3. On the other hand, the sheet concentration of boron at the same interface was 5E10 atoms/cm^2. As in the previous embodiments, these results were obtained using the above-mentioned secondary-ion mass spectroscopic (SIMS) technique and are plotted in Fig. 13.

Finally, a fifth embodiment of the present invention will be described with reference to Figs. 11 and 12. In the fifth embodiment, the boron isolating means such as the clean work station 110 of Figs. 5(A) and 5(B) is used as in the first embodiment. As shown in Fig. 12, the fifth embodiment uses only one growth chamber (denoted by numeral 39).

It is assumed that the silicon substrates (or wafers), on each of which the layers shown in Fig. 1(A) has already been formed, are pretreated and then transferred to an UHV-CVD apparatus (or system) 31 shown in Fig. 12.

In Fig. 11, steps 500 to 512 are respectively identical with steps 80 to 92 and accordingly, they will not been described for the sake of brevity. At step 514, the temperature of the wafer is raised to about 700°C, after which the growth chamber 39 is cleaned while flowing an F_2 gas (flow rate is 20 sccm) for about 5 minutes. Accordingly, baron residues (solid) an the inner wall of the growth chamber 39 are vaporized as shown below.

$$2B\ (solid) + 3F_2\ (gas) \rightarrow 2BF_3\ (gas)$$

The $2BF_3$ gas is evacuated outside the chamber 39. After cleaning the growth chamber 39, a first wafer is loaded into the chamber 39 from the load-lock chamber 34a at step 516. The wafer is then subjected to a high-temperature flashing in order to remove native oxide formed thereon at step 518. Thereafter, at step 520, a non-doped epitaxial growth (2000 angstrom (for example)) on the wafer is implemented in the chamber 39. Subsequently, at the same chamber 39, a boron-doped epitaxial growth (2000 angstrom (for example)) is carried out on the non-doped layer while flowing Si_2H_6 and (H_2(1%) + B_2H_6 (99%)) both at a flow rate of 10 sccm. When the non- and boron-doped epitaxial growths are completed, the wafer is transferred to the load-lock chamber 34b (step 522). The flow goes back to step 514 whereat the next wafer is subjected to the above mentioned processes at steps 514 to 522. At step 524, a check is made to determine if all the wafers stored in the load-lock chamber 34a have been processed. If the answer is positive (viz., YES), the routine is terminated.

In connection with the fifth embodiment, the inventors conducted an experiment under the aforesaid conditions. Although not shown in Fig. 13, the experiment results showed that the peak concentration of boron at an interface between the epitaxial layer and the substrate was 4E16 atoms/cm^3. On the other hand, the sheet concentration of boron at the same interface was 1E11 atoms/cm^2. As in the previous embodiments, these results were obtained using the above-mentioned secondary-ion mass spectroscopic (SIMS) technique.

It will be understood that the above disclosure is representative of five possible embodiments of the present invention and that the concept on which the invention is based is not specifically limited thereto,

Claims

1. A method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of:

   (a) cleaning the substrate using a solution including a plurality of chemicals each of which contains boron whose concentration is less than 50 ppt, said cleaning being implemented before the substrate is loaded into the CVD apparatus; and
   (b) processing the substrate in a boron-free isolated environment at step (a) and before the substrate is loaded into the CVD apparatus.

2. A method as claimed in claim 1, wherein said processing of the substrate at step (b) further includes washing the substrate with water, drying the substrate, transferring the substrate to the CVD apparatus, and loading the substrate into the CVD apparatus.

3. A method as claimed in claim 2, wherein said transferring of the substrate to the CVD apparatus is implemented using a substrate carry box filled with nitrogen.

4. A method as claimed in claim 1, wherein said boron-free isolated environment is provided in a clean room which contains boron resulting from a glass fiber filter.

5. A method as claimed in claim 4, wherein said transferring of the substrate to the CVD apparatus is implemented using a substrate carry box filled with nitrogen.

6. A method as claimed in claim 1, wherein the solution for cleaning the substrate at step (a) is composed of NH_4OH-H_2O_2-H_2.

7. A method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of:

   (a) ion implanting silicon atoms into the substrate before the substrate is loaded into the CVD apparatus;
   (b) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus; and
   (c) implementing a high-temperature treatment on the substrate in the CVD apparatus thereby diffusing boron, adhered to the substrate, into the substrate.

8. A method as claimed in claim 7, wherein said high-temperature treatment in step (c) removes native oxide, produced on the substrate in an ambient clean room atmosphere, during the cleaning of the substrate.

9. A method as claimed in claim 7, further comprising the steps of:

   (d) thermally growing oxide on the substrate before step (a); and
   (e) completely removing the thermally grown oxide between steps (a) and (b).

10. A method as claimed in claim 7, the solution used at step (b) is composed of NH_4OH-H_2O_2-H_2.

11. A method as claimed in claim 7, wherein the substrate is transferred to the CVD apparatus using a substrate carry box filled with nitrogen.

12. A method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of:

(a) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus;
(b) removing native oxide produced on the substrate at step (a) using a dilute HF before the substrate is loaded into the CVD apparatus;
(c) immersing the substrate in boiling concentrated HNO_3 to form native oxide on the substrate, the immersing of the substrate being implemented before the substrate is loaded into the CVD apparatus; and
(d) implementing a high-temperature treatment on the substrate in the CVD apparatus to diffuse boron, adhered to the substrate, into the substrate.

13. A method as claimed in claim 12, further comprising the step of:

(e) reducing the thickness of the native oxide, produced in step (c), using a dilute HF to a predetermined value before the substrate is loaded into the CVD apparatus, the dilute HF used in step (e) having concentration lower than the dilute HF used at step (b).

14. A method as claimed in claim 12, wherein the substrate is transferred to the CVD apparatus using a substrate carry box filled with nitrogen.

15. A method as claimed in claim 12, the solution used at step (a) is composed of NH_4OH-H_2O_2-H_2.

16. A method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of:

(a) cleaning the substrate using a solution including H_2O_2 before the substrate is loaded into the CVD apparatus;
(b) removing native oxide produced on the substrate at step (a) using a dilute HF before the substrate is loaded into the CVD apparatus;
(c) growing thermally oxide on the substrate using an oxygen gas in a low-pressure atmosphere before the substrate is loaded into the CVD apparatus; and
(d) implementing a high-temperature treatment on the substrate in the CVD apparatus to remove the oxide which has thermally been grown on the substrate at step (c).

17. A method as claimed in claim 16, wherein the thermal oxide growth at step (c) is implemented at less than 20 torr in a CVD growth chamber with the temperature of the substrate being equal to or less than 900°C, and wherein the thermal oxide grown at step (c) has a thickness of being equal to or less than 30 angstrom.

18. A method as claimed in claim 16, wherein the substrate is transferred to the CVD apparatus using a substrate carry box filled with nitrogen.

19. A method as claimed in claim 16, the solution used at step (a) is composed of NH_4OH-H_2O_2-H_2.

20. A method of reducing boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, comprising the steps of;

(a) cleaning a CVD growth chamber, before the substrate is loaded into the growth chamber, using an F_2 gas at a predetermined temperature of the substrate, thereby to remove boron residues in the growth chamber;
(b) implementing a high-temperature treatment on the substrate loaded into the growth chamber to remove native oxide on the substrate; and
(c) implementing sequentially non-doped and boron-doped epitaxial growths on the substrate in the growth chamber.

21. A method as claimed in claim 20, further comprising the steps;

(d) cleaning the substrate using a solution including a plurality of chemicals each of which contains boron whose concentration is less than 50 ppt, said cleaning being implemented before the silicon substrate is loaded into the CVD apparatus; and
(e) processing the substrate in a boron-free isolated environment at step (d) and before the substrate is loaded into the CVD apparatus.

22. A method as claimed in claim 21, wherein said processing of the substrate at step (e) further includes washing the substrate with water, drying the substrate, transferring the substrate to the CVD apparatus, and loading the substrate into the CVD apparatus.

23. A method as claimed in claim 22, wherein said transferring of the substrate to the CVD apparatus is implemented using a substrate carry box filled with nitrogen.

24. A method as claimed in claim 21, wherein said boron-free isolated environment is provided in a clean room wherein boron resulting from a glass fiber filter is contained.

25. A method as claimed in claim 24, wherein said transferring of the substrate to the CVD apparatus is implemented using a substrate carry box filled with nitrogen.

26. A method as claimed in claim 21, wherein said solution for cleaning the substrate at step (a) is composed of NH_4OH-H_2O_2-H_2.

FIG. 1(A)
(PRIOR ART)

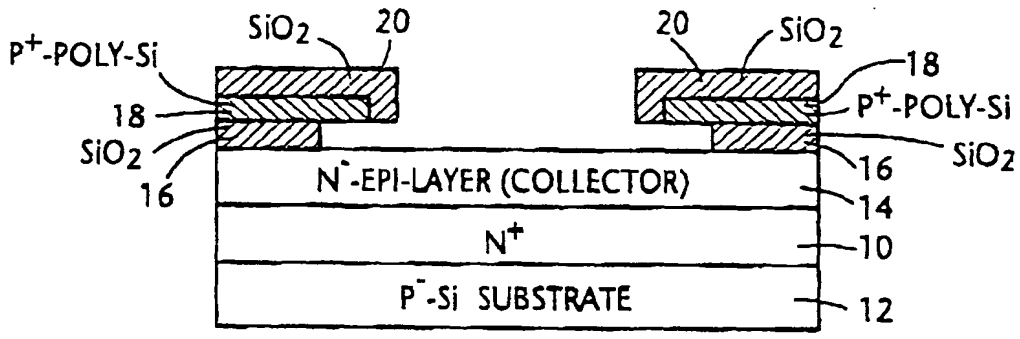


FIG. 1(B)
(PRIOR ART)

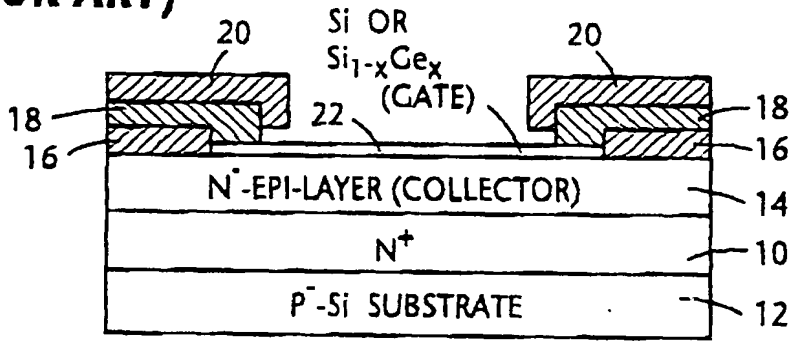


FIG. 1(C)
(PRIOR ART)

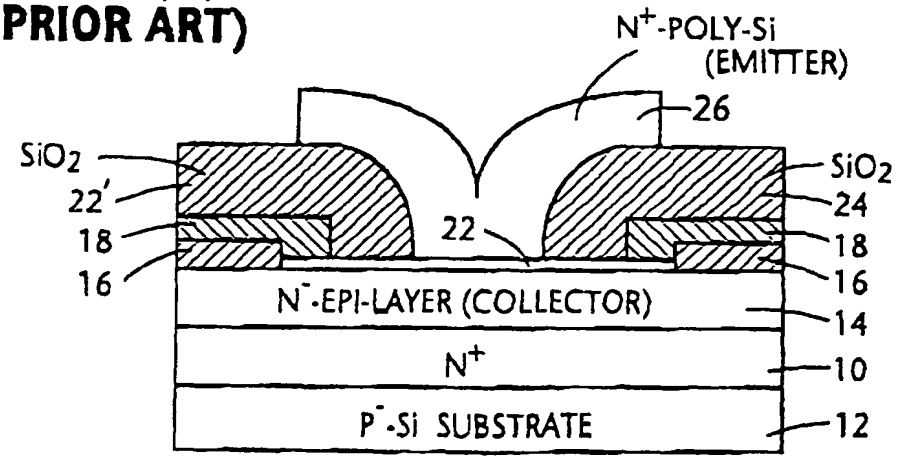


FIG. 2 (PRIOR ART)

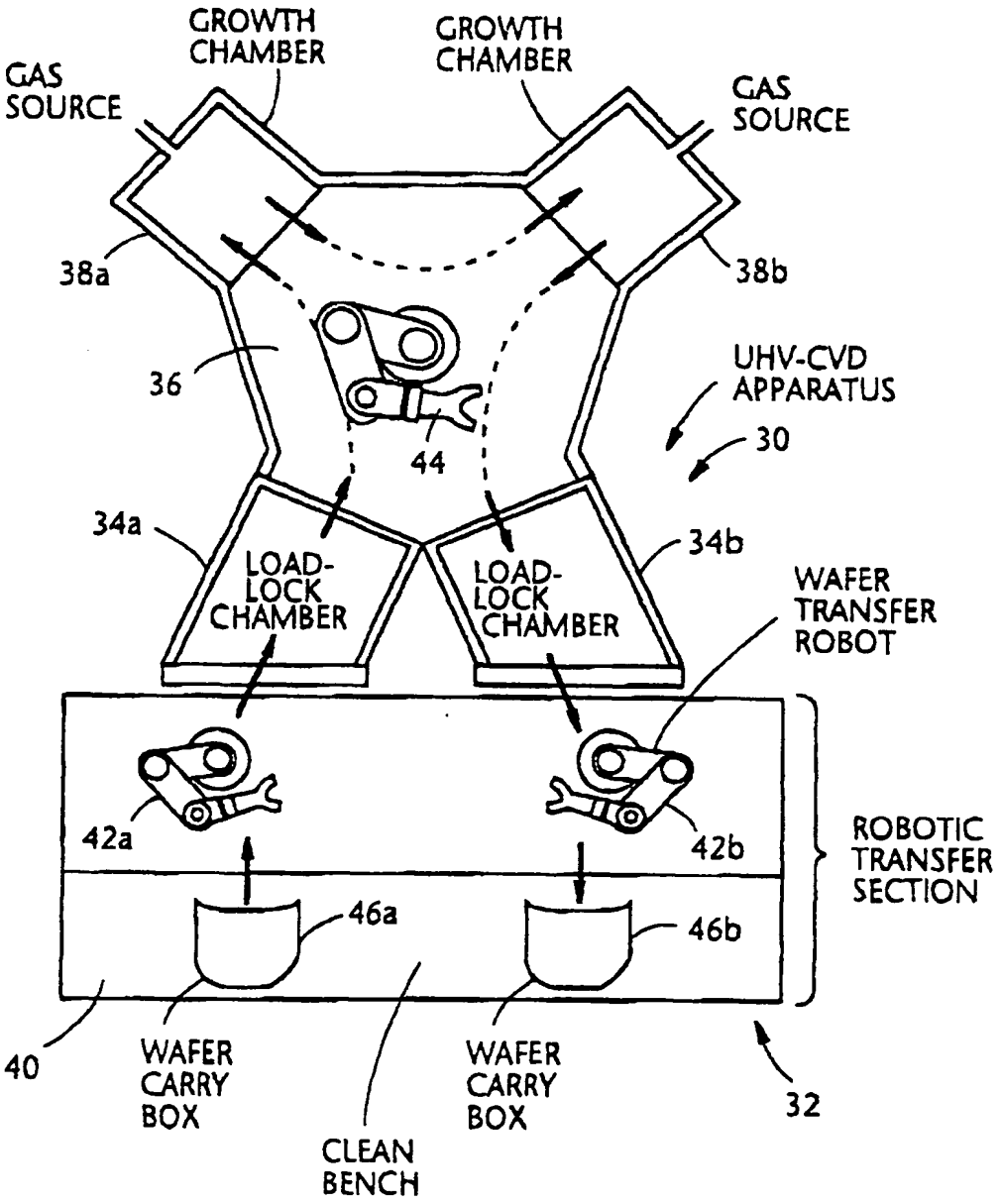


FIG. 3
(PRIOR ART)

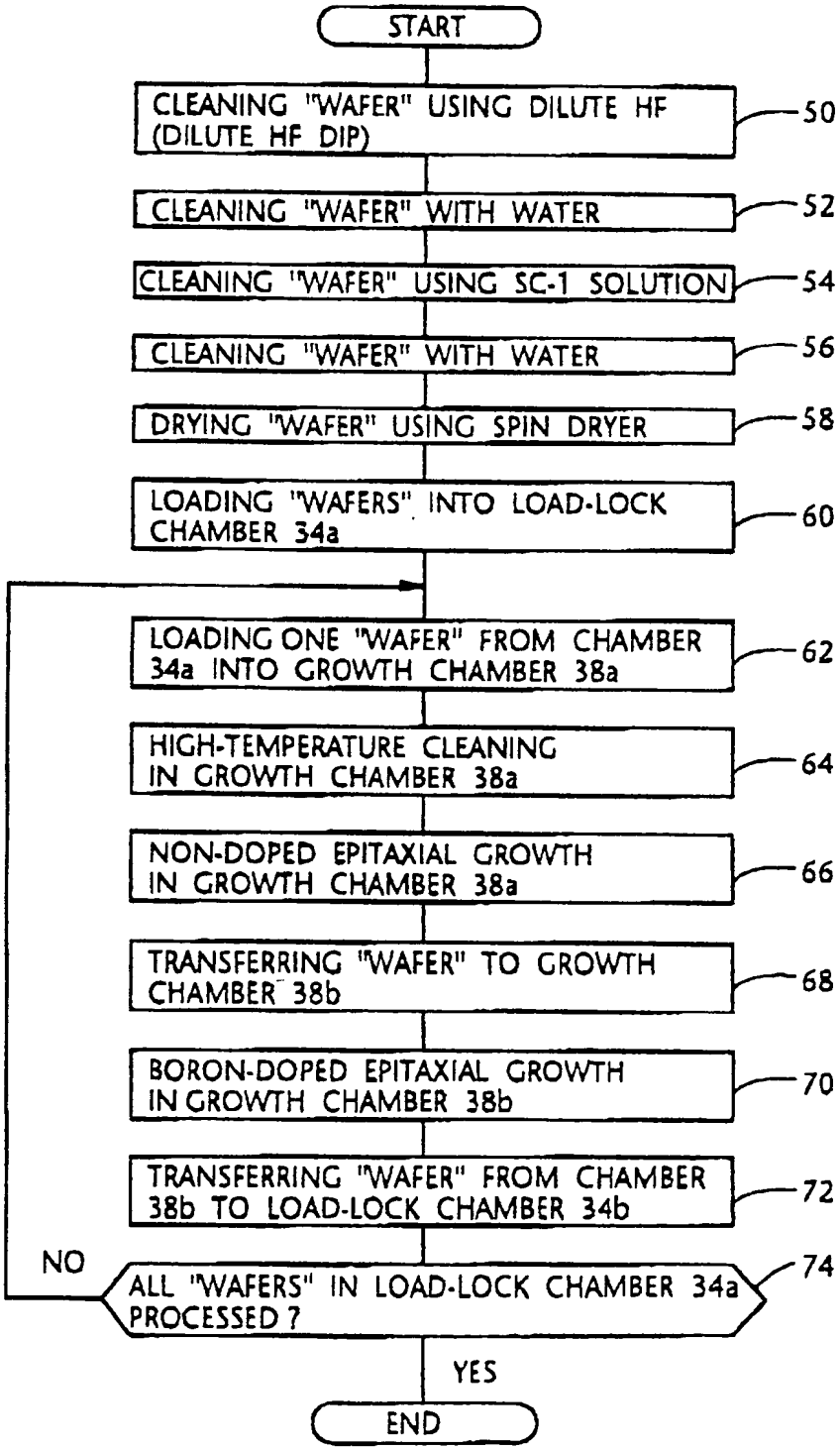


FIG. 4

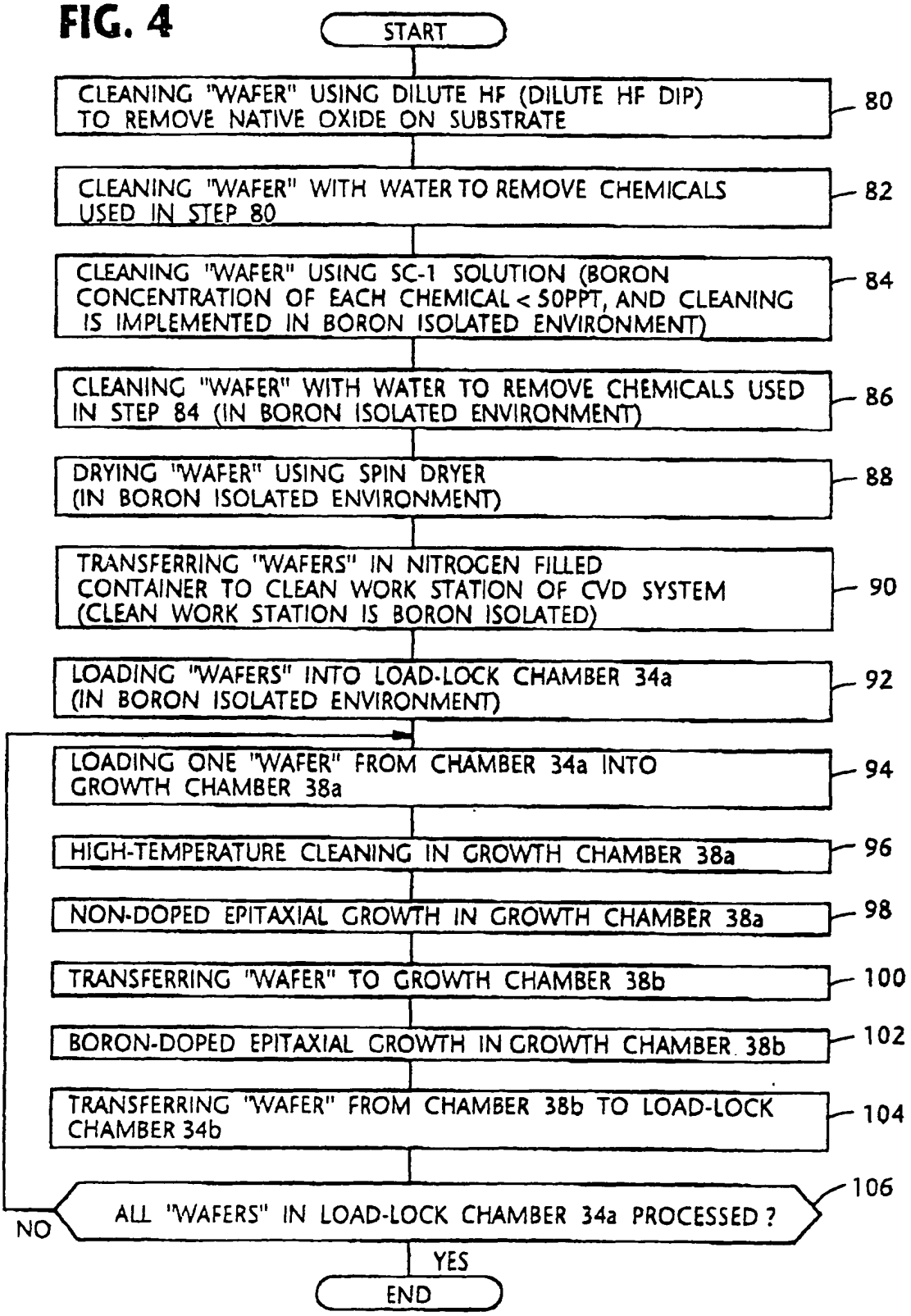


FIG. 5A

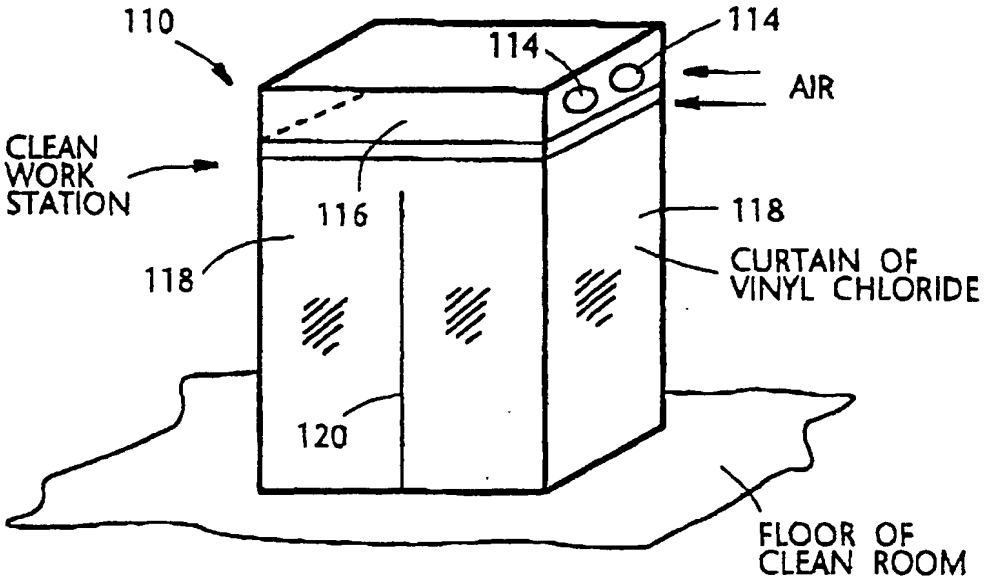


FIG. 5B

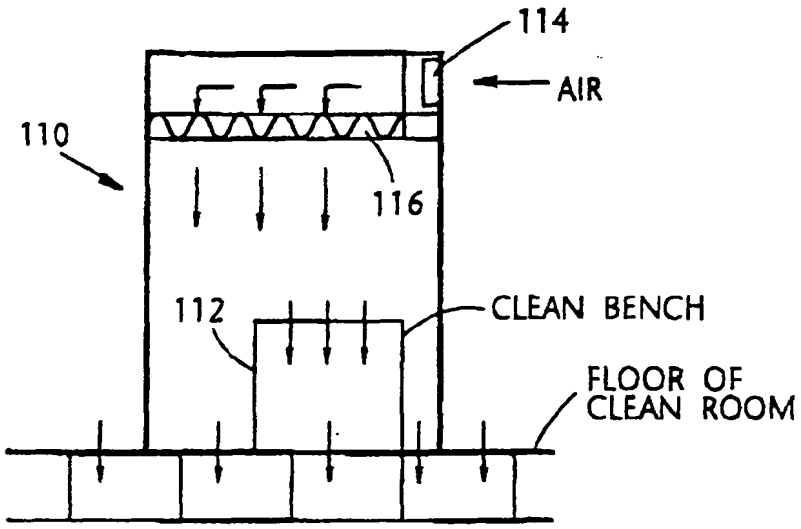


FIG. 6

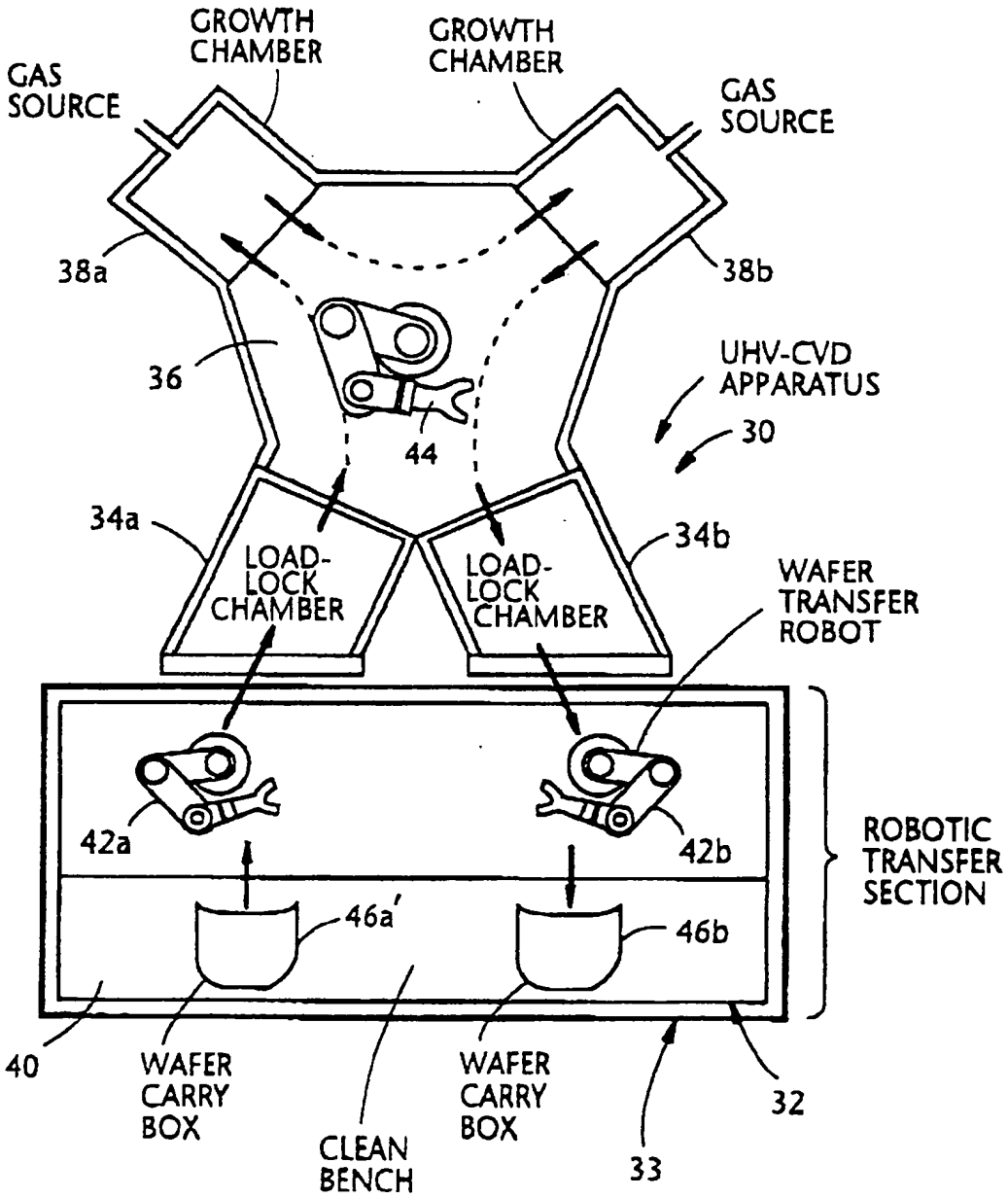


FIG. 7

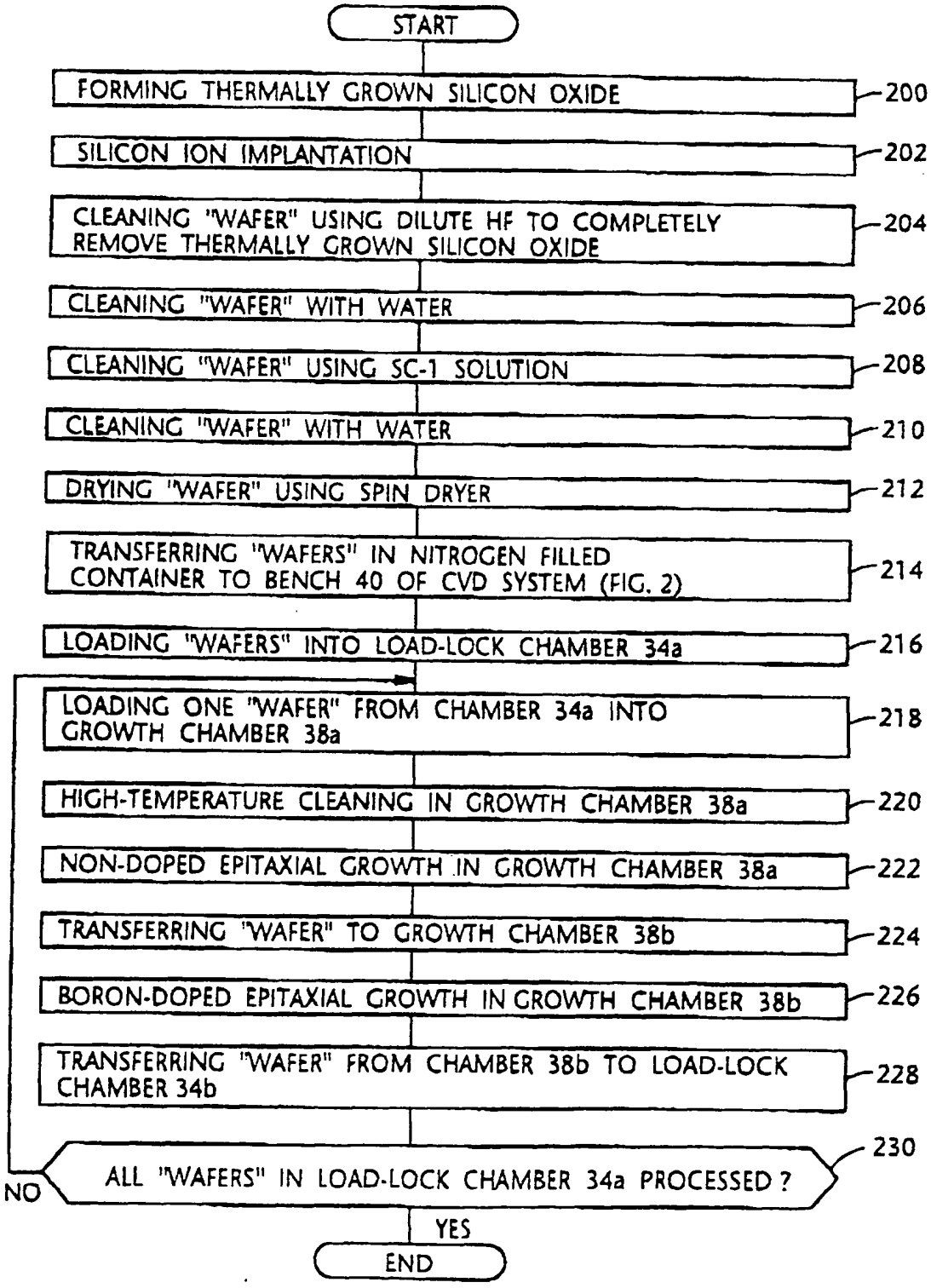


FIG. 8(A)

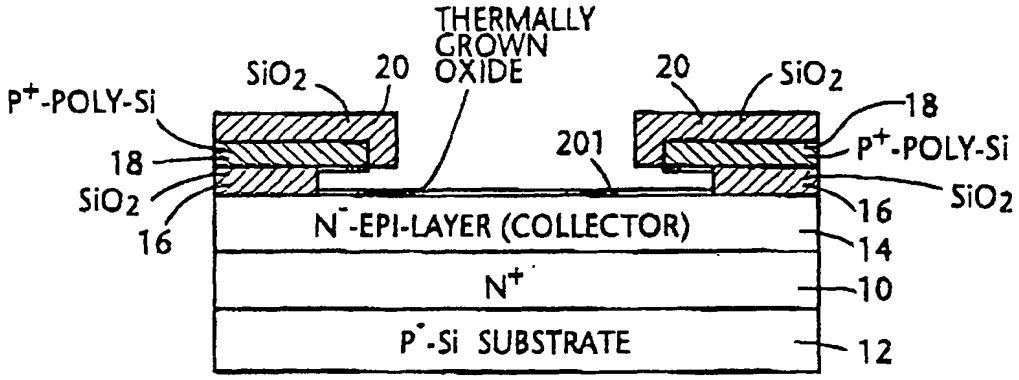


FIG. 8(B)

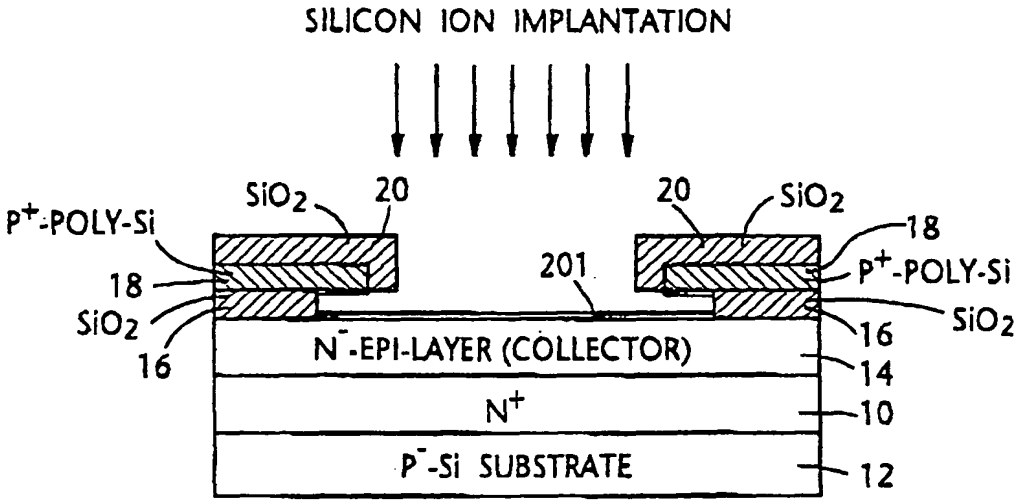


FIG. 9(A)

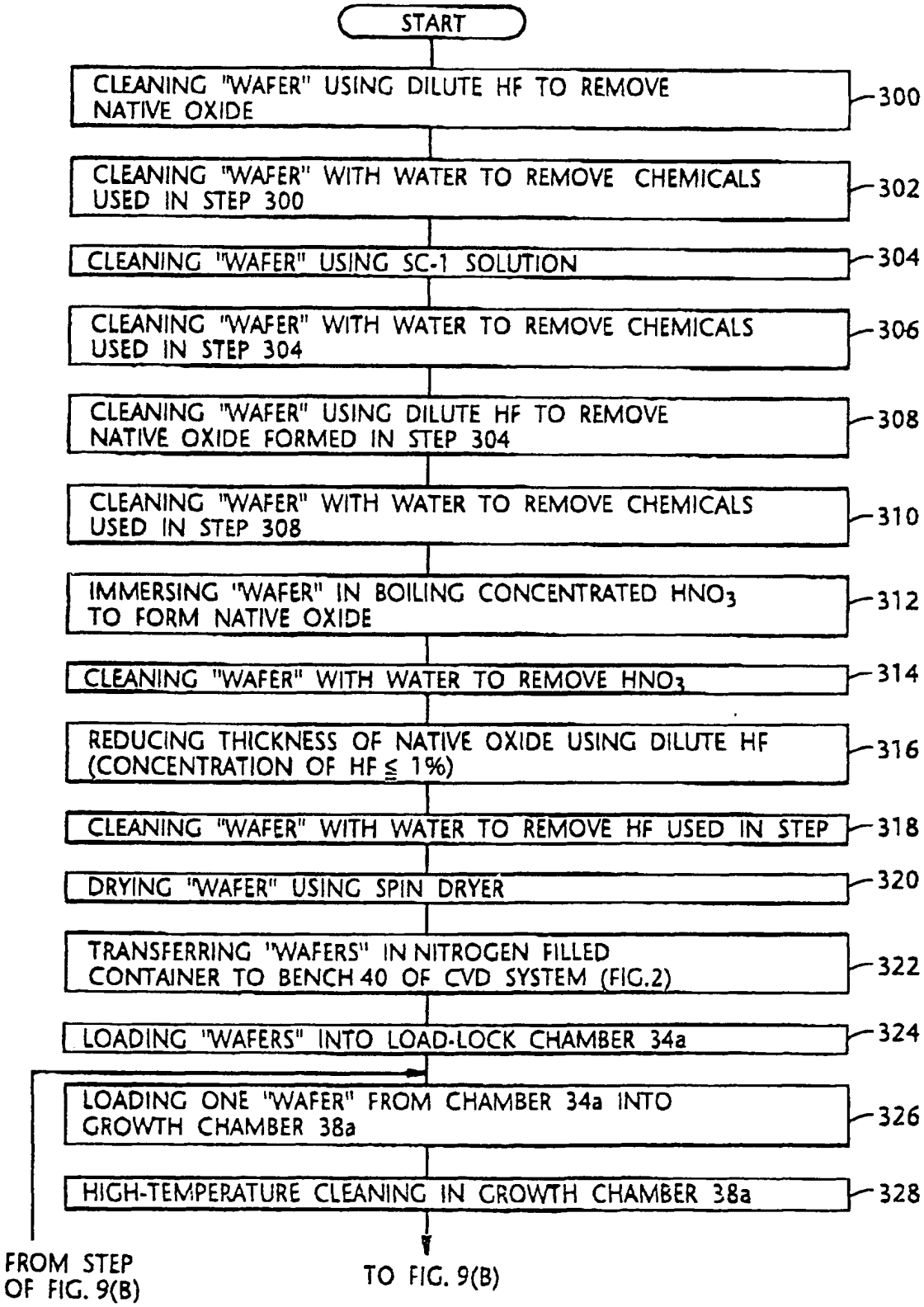


FIG. 9(B)

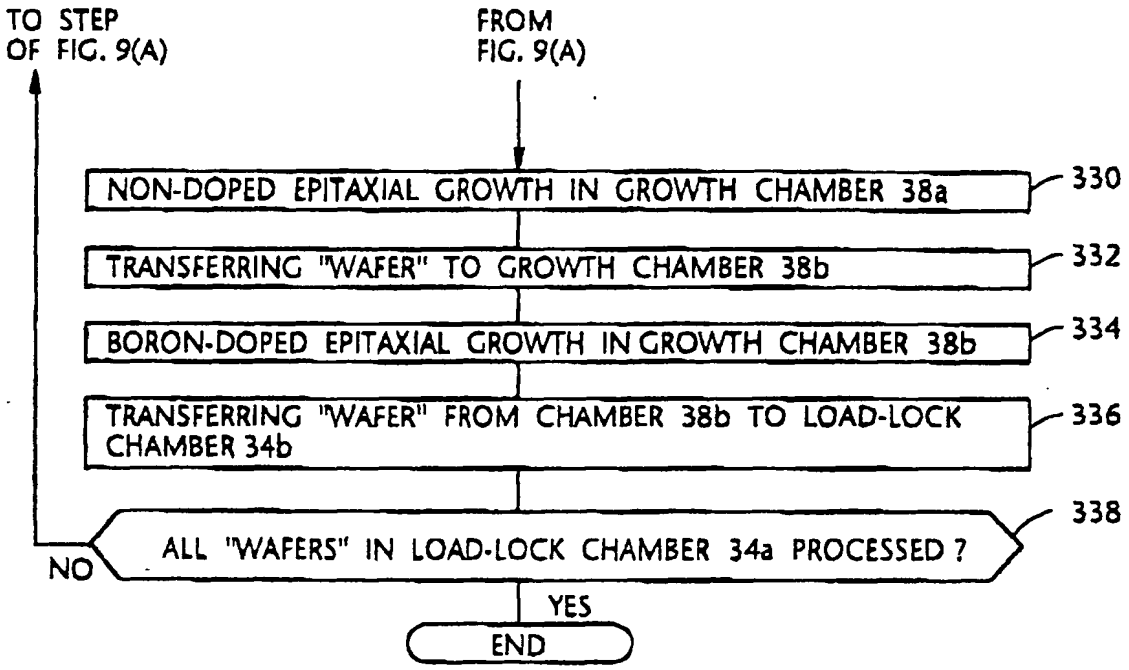


FIG. 10

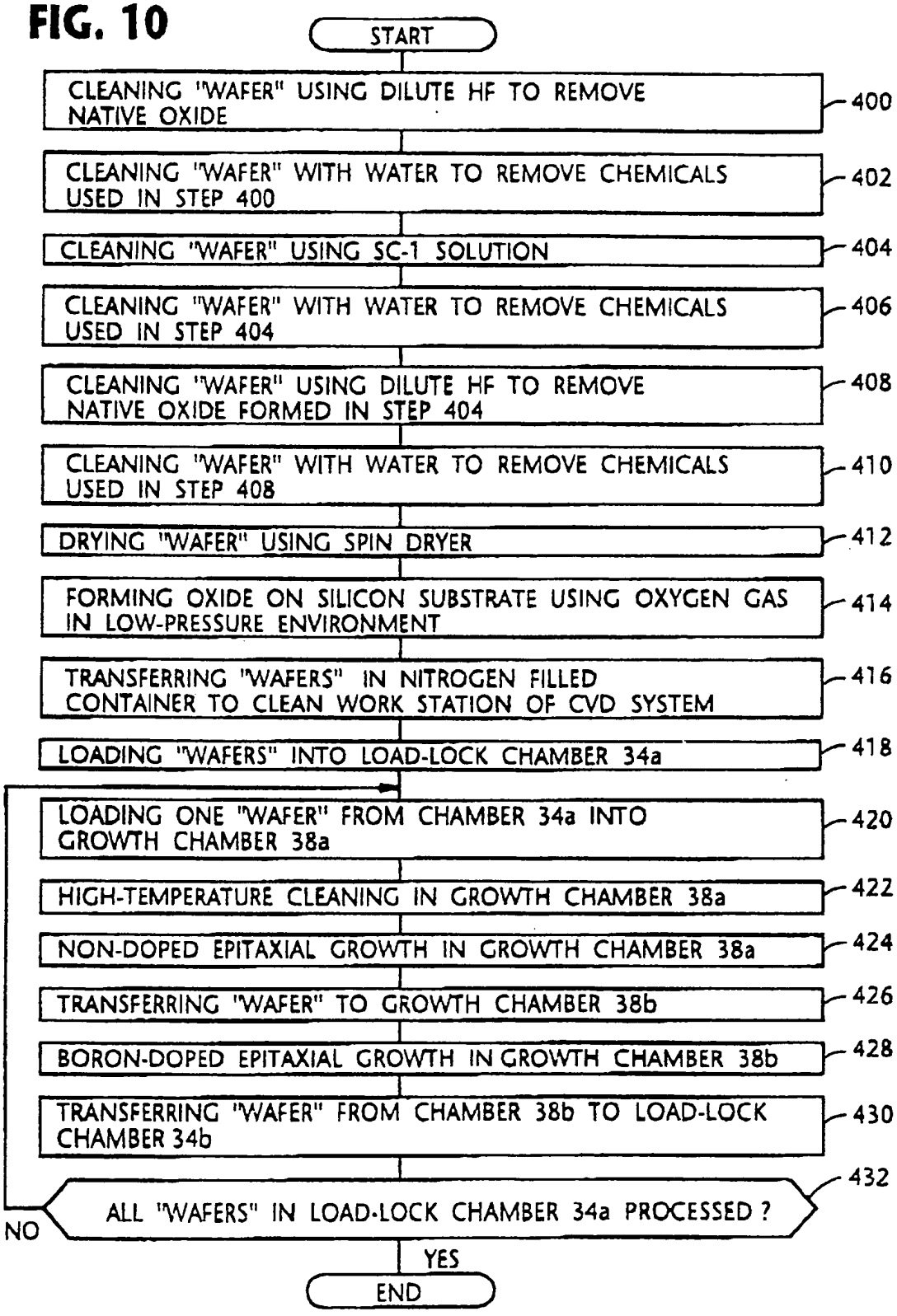


FIG. 11

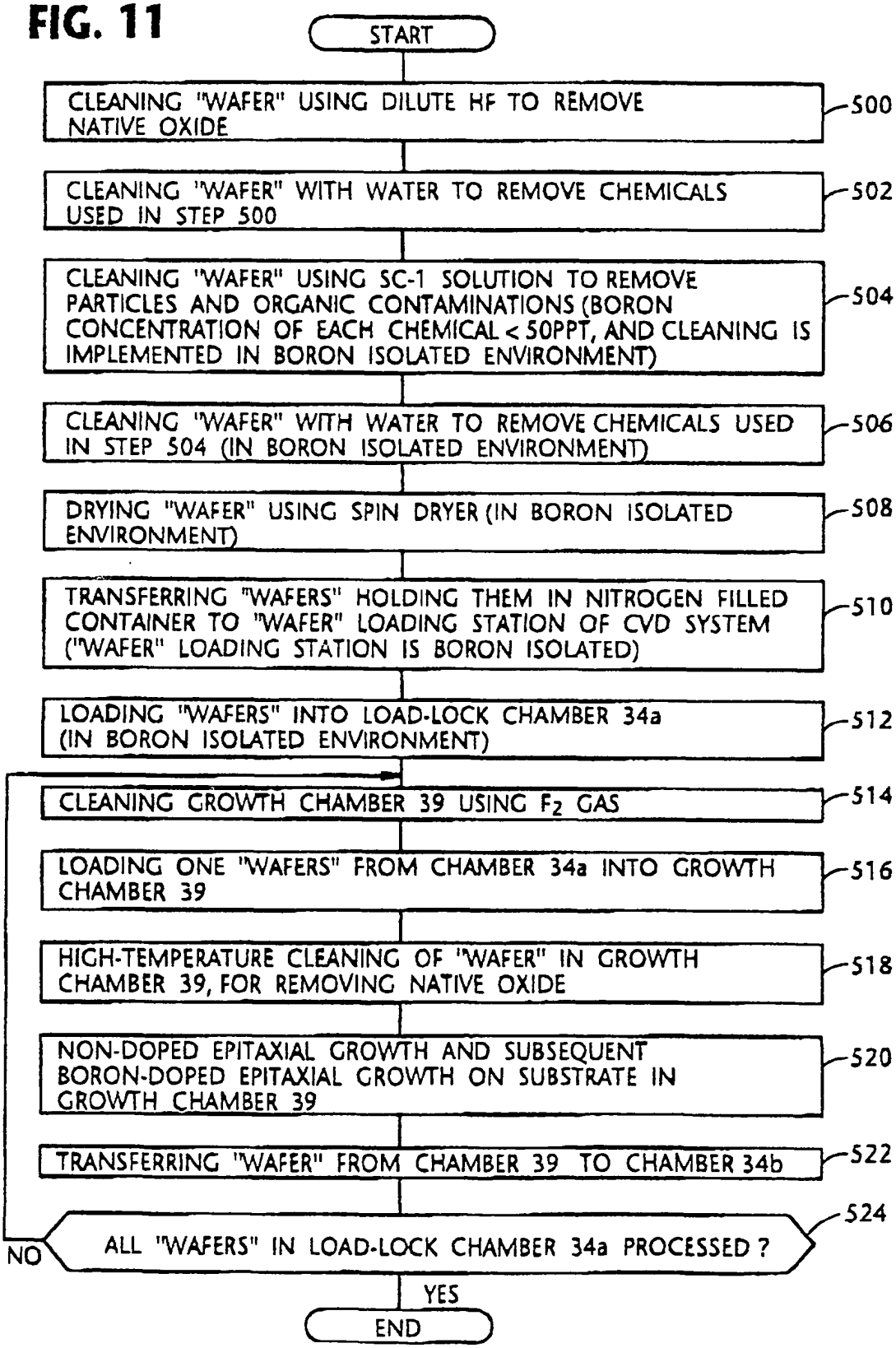


FIG. 12

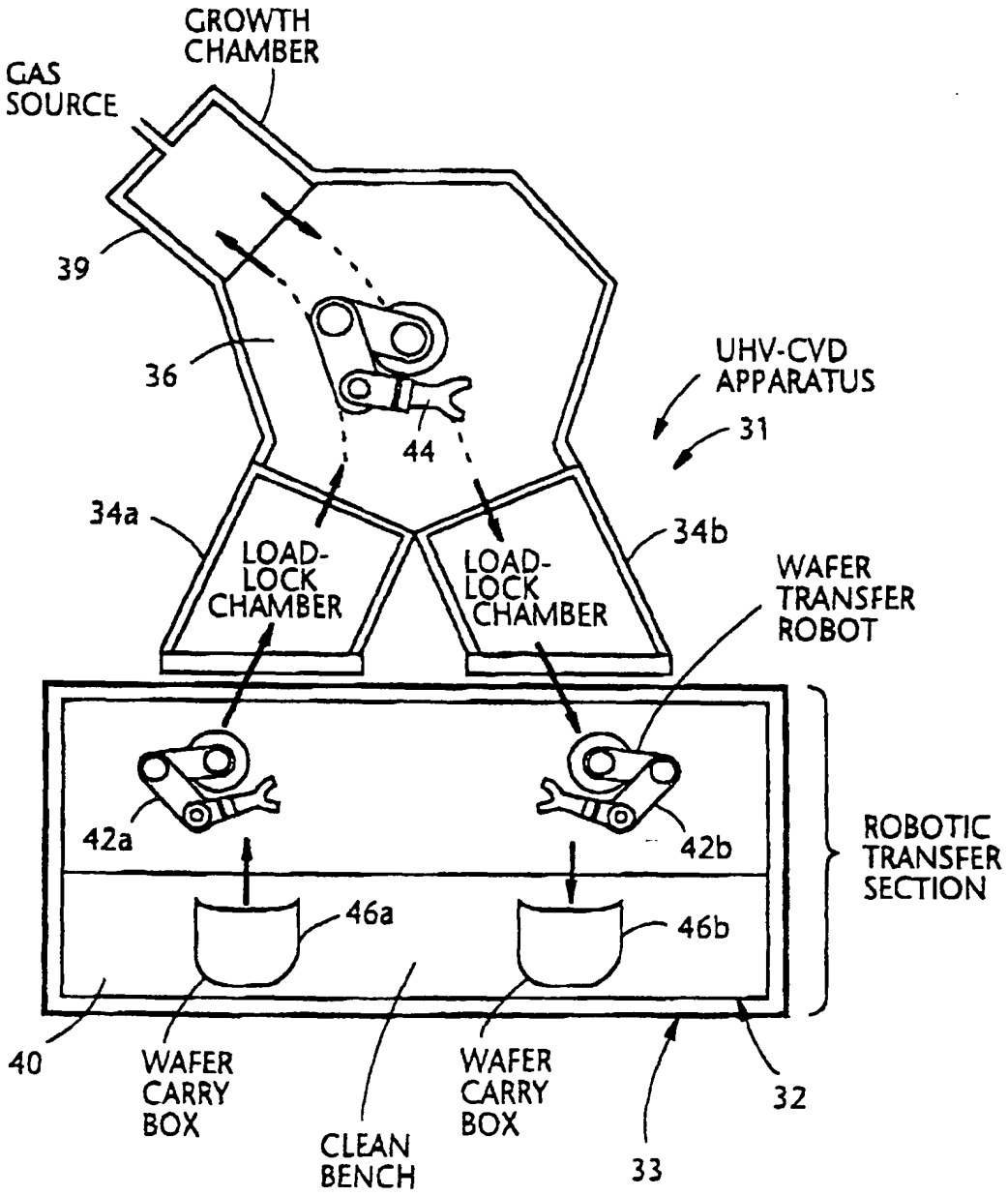
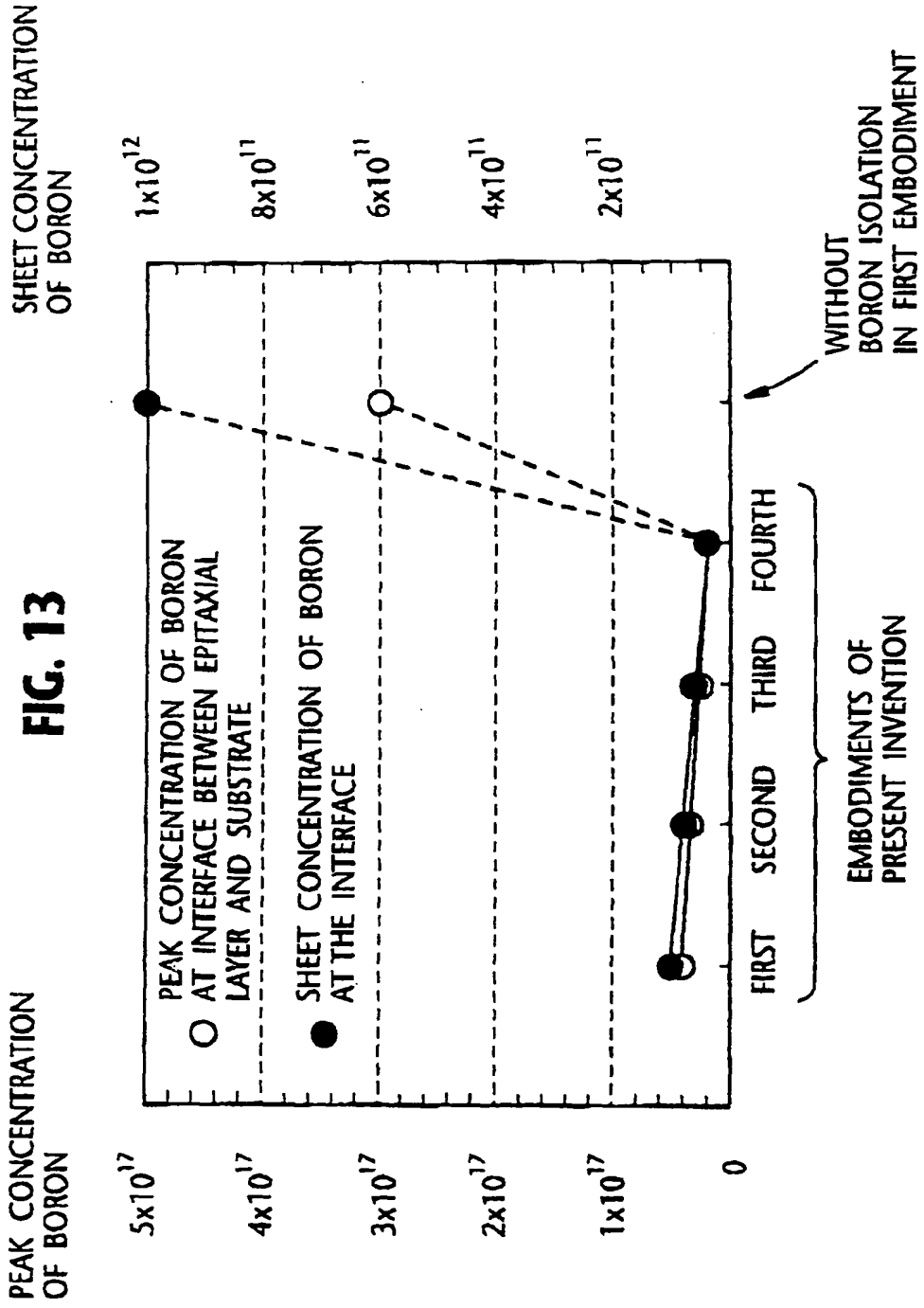


FIG. 13



(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 844 649 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
06.10.1999 Bulletin 1999/40

(43) Date of publication A2:
27.05.1998 Bulletin 1998/22

(21) Application number: **97120374.0**

(22) Date of filing: **20.11.1997**

(51) Int. Cl.[6]: **H01L 21/306**, H01L 21/205

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **20.11.1996 JP 30884296**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

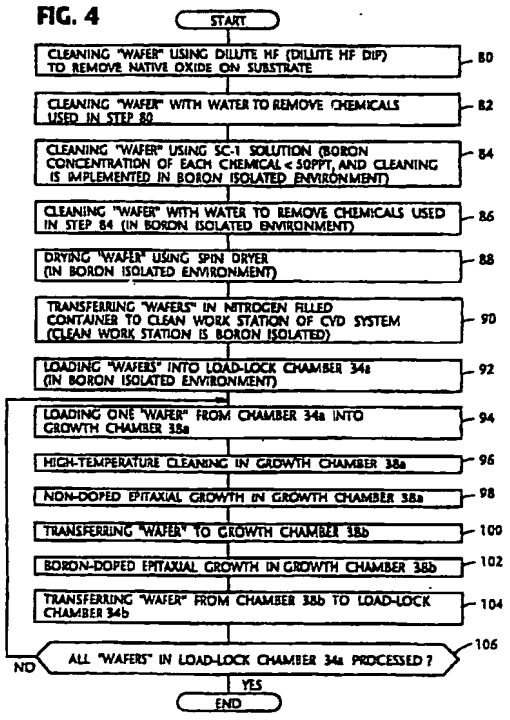
(72) Inventors:
- **Suzuki, Tatsuya**
  Minato-ku, Tokyo (JP)
- **Aoyama, Tohru**
  Minato-ku, Tokyo (JP)

(74) Representative:
Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) A method for boron contamination reduction in IC fabrication

(57) In order to reduce boron concentration between a silicon substrate and an Si or $Si_{1-x}Ge_x$ layer which is epitaxially grown in a CVD (chemical vapor deposition) apparatus, the silicon substrate is pre-treated, before being loaded into the CVD apparatus, such as to prevent the substrate from being contaminated by boron in a clean room. Further, in accordance with one embodiment, a CVD growth chamber itself is cleaned, before the substrate is loaded into the growth chamber, using an F_2 gas at a predetermined temperature of the substrate, thereby to remove boron residues in the growth chamber;

FIG. 4



EP 0 844 649 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 12 0374

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	CAYMAX M R ET AL: "Optimization of Si-wafer cleaning and the use of buffer-layers for epitaxial growth of SiGe-layers by VLPCVD at T=650 C" CHEMICAL SURFACE PREPARATION, PASSIVATION AND CLEANING FOR SEMICONDUCTOR GROWTH AND PROCESSING SYMPOSIUM, SAN FRANCISCO, CA, 27 - 29 April 1992, pages 461-466, XP002111368 1992, Pittsburgh, PA, USA, Mater. Res. Soc, USA * the whole document * ---	1-6	H01L21/306 H01L21/205
A	STEVIE F A ET AL: "Boron contamination of surfaces in silicon microelectronics processing: characterization and causes" TOPICAL CONFERENCE ON THE PROCESSED INDUCED PARTICULATE CONTAMINATION, TORONTO, ONT., CANADA, 8. OCT. 1990, vol. 9, no. 5, pages 2813-2816, XP002111369 Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), Sept.-Oct. 1991, USA ISSN: 0734-2101 * the whole document * ---	1,3,4, 12,16	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L C23C
A	HASHIMOTO T ET AL: "Boron spike effect on cut-off frequency and early voltage in SiGe HBTs" ESSDERC '95. PROCEEDINGS OF THE 25TH EUROPEAN SOLID STATE DEVICE RESEARCH CONFERENCE, THE HAGUE, NETHERLANDS, 25 - 27 September 1995, pages 501-504, XP002111370 1995, Gif sur Yvette, France, Editions Frontieres, France ISBN: 2-86332-182-X * the whole document * --- -/--	7,8,12	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 August 1999	Köpf, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 12 0374

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	IYER S S ET AL: "Origin and reduction of interfacial boron spikes in silicon molecular beam epitaxy" APPLIED PHYSICS LETTERS, vol. 52, no. 6, 8 February 1988 (1988-02-08), pages 486-488, XP002111371 ISSN: 0003-6951 * the whole document *	7	
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 302 (C-616), 12 July 1989 (1989-07-12) & JP 01 093412 A (IWATANI INTERNATL CORP), 12 April 1989 (1989-04-12) * abstract *	20	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 August 1999	Köpf, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 12 0374

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

05-08-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 01093412 A	12-04-1989	JP 1922568 C	07-04-1995
		JP 6045455 B	15-06-1994

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82